IN THE CLAIMS

1. (Original) A phase locked loop circuit, for providing an oscillating output signal at an output frequency, comprising:
a reference counter;
a loop counter;
a phase detector having a first input coupled to the reference counter and a second input coupled to the loop counter;
a voltage controlled oscillator having an input coupled to the output of the phase detector and an output for providing the oscillating output signal;
a feedback loop coupling the output of the voltage controlled oscillator to the input of the loop counter; and
delay circuitry, including a feedback loop, arranged to introduce a discrete delay into the output of the loop counter and/or the reference counter.

2. (Original) A phase locked loop circuit as claimed in claim 1, wherein the delay circuit temporarily introduces an off-set into the loop counter and/or the reference counter.

3. (Currently Amended) A phase locked loop circuit as claimed in claim 1 ~~or 2~~, wherein the delay circuit comprises a variable delay component for introducing a continuously variable delay into the output of the loop counter and/or the reference counter.

4. (Currently Amended) A phase locked loop circuit as claimed in claims 3, wherein the delay circuitry comprises a detector for detecting when the variable delay component exceeds a threshold and control means for introducing a discrete delay in response to said detection.

5. (Currently Amended) A phase locked loop circuit as claimed in claim 3 ~~or 4~~, wherein the delay circuit is arranged to compensate a variation in the discrete delay with a variation in the variable delay.

6. (Currently Amended) A phase locked loop circuit as claimed in claim 3, ~~4 or 5,~~ wherein the delay circuitry is arranged such that a maximum variable delay is substantially equal to a minimum discrete delay.

7. (Currently Amended) A phase locked loop circuit as claimed in ~~any one of~~ claims 3 ~~to~~ 6, wherein the delay circuitry comprises a feedback loop which provides an input to the variable delay component that is dependent upon both the voltage at the input to the voltage controlled oscillator and the discrete delay introduced into the loop counter and/or the reference counter.

8. (Original) A phase locked loop circuit as claimed in claim 7, wherein the delay circuit temporarily introduces an off-set into the loop counter and/or the reference counter and comprises: a summation means for summing the introduced offsets; a digital to analogue conversion means for converting the total introduced offset into an analogue signal representing the total introduced discrete delay; and subtraction means for subtracting the analogue signal from a signal representative of the voltage at the input of the voltage controlled oscillator to produce the input to the variable delay component.

9. (Currently Amended) A phase locked loop circuit as claimed in ~~any preceding~~ claim 1, further comprising a shunt capacitor connected between a node between the phase detector and the voltage controlled oscillator and ground.

10. (Currently Amended) A phase locked loop circuit as claimed in ~~any preceding~~ claim 1, wherein the phase detector output is coupled to the input of the voltage controlled oscillator via an intervening loop filter consisting of a capacitor.

11. (Currently Amended) A frequency synthesiser comprising a phase locked loop circuit as claimed in ~~any preceding~~ claim 1.

12. (Original) A method of changing the frequency of an oscillating output signal comprising the steps of:
adapting the reference counter and/or the loop counter of a phase locked loop; and introducing a discrete delay into the output of the loop counter and/or the reference counter.

13. (Original) A method as claimed in claim 12 further comprising the step of introducing a continuously variable delay into the output of the loop counter and/or the reference counter.

14. (Original) A method as claimed in claim 13, wherein a temporary variation of the discrete delay results in a corresponding permanent variation in the variable delay.

15. (Original) A frequency synthesiser, for providing an oscillating output signal at an output frequency, comprising:
frequency compensation means arranged to maintain the output frequency; and
feedback means arranged to vary discretely the phase of an input signal provided to the compensation means.

16. (Original) A frequency synthesiser as claimed in claim 15, wherein the feedback means is additionally arranged to vary continuously the phase delay of the input signal.

17. (Original) A frequency synthesiser as claimed in claim 15, wherein the compensation means comprises: an input for receiving a first input signal; comparison means for comparing the first input signal and a second input signal; control means for controlling the output frequency in dependence upon the comparison; and a negative feedback loop for providing the second input signal.

18. (Original) A frequency synthesiser as claimed in claim 17, wherein the comparison means is a phase detector.

19. (Currently Amended) A frequency synthesiser as claimed in claim 17 ~~or 18~~, wherein the control means comprises a capacitor, a voltage controlled oscillator having its input connected to the capacitor and means for sourcing and sinking current to said capacitor and thereby control the output of said voltage controlled oscillator and the output frequency.

20. (Currently Amended) A frequency synthesiser as claimed in ~~any one of~~ claim~~s~~ 17, ~~18 or 19,~~ wherein the negative feedback loop comprises programmable means for adjusting the second input signal.

21. (Original) A frequency synthesiser as claimed in claim 20, wherein the programmable means is a counter.

22. (Currently Amended) A frequency synthesiser as claimed in ~~any one of~~ claims 17 ~~to~~ ~~21~~, wherein the feedback means is additionally arranged to continuously vary the phase delay of the first input signal.

23. (Currently Amended) A frequency synthesiser as claimed in ~~any one of~~ claims 17 ~~to~~ ~~21~~, wherein the feedback means is additionally arranged to continuously vary the phase delay of the second input signal.

24. (Currently Amended) A frequency synthesiser as claimed in claim 22 ~~or 23~~, wherein the feedback means comprises a negative feedback loop.

25. (Original) A phase locked loop circuit, for providing an oscillating output signal at an output frequency, comprising:
a loop counter;
a phase detector having a first input coupled to the reference counter and a second input coupled to the loop counter;
a voltage controlled oscillator having an input coupled to the output of the phase detector and an output for providing the oscillating output signal;
a feedback loop coupling the output of the voltage controlled oscillator to the input of the loop counter; and
delay circuitry, including a feedback loop, arranged to introduce a discrete delay into the output of the loop counter.

26. (Original) A method of changing the frequency of an oscillating output signal comprising the steps of:
adapting a loop counter of a phase locked loop; and
using a feedback loop to introduce a discrete delay into the output of the loop counter.

27. (Original) A frequency synthesiser, for providing an oscillating output signal at an output frequency, comprising:
frequency compensation means comprising: an input for receiving a first input signal; comparison means for comparing the first input signal and a second input signal; control means for controlling the output frequency in dependence upon the comparison; and a negative feedback loop for providing the second input signal; and feedback means

arranged to vary discretely the phase of the first input signal and to vary continuously the phase of the first input signal.

28. (Original) A frequency synthesiser as claimed in claim 27, wherein the comparison means is a phase detector.

29. (Currently Amended) A frequency synthesiser as claimed in claim 27 ~~or 28~~, wherein the control means comprises a capacitor, a voltage controlled oscillator having its input connected to the capacitor and means for sourcing and sinking current to said capacitor and thereby control the output of said voltage controlled oscillator and the output frequency.

30. (Currently Amended) A frequency synthesiser as claimed in ~~any one of~~ claim~~s~~ 27, ~~28 or 29,~~ wherein the negative feedback loop comprises programmable means for adjusting the second input signal.

31.(Original) A frequency synthesiser as claimed in claim 30, wherein the programmable means is a counter.

32. (Original) A frequency synthesiser, for providing an oscillating output signal at an output frequency, comprising:
frequency compensation means comprising: an input for receiving a first input signal; comparison means for comparing the first input signal and a second input signal; control means for controlling the output frequency in dependence upon the comparison; and a negative feedback loop for providing the second input signal; and feedback means arranged to vary discretely the phase of the second input signal and to vary continuously the phase delay of the second input signal.

33. (Original) A frequency synthesiser as claimed in claim 32, wherein the comparison means is a phase detector.

34. (Currently Amended) A frequency synthesiser as claimed in claim 32 ~~or 33~~, wherein the control means comprises a capacitor, a voltage controlled oscillator having its input connected to the capacitor and means for sourcing and sinking current to said capacitor and thereby control the output of said voltage controlled oscillator and the output

frequency.

35. (Currently Amended) A frequency synthesiser as claimed in ~~any one of~~ claim~~s~~ 32, ~~33 or 34,~~ wherein the negative feedback loop comprises programmable means for adjusting the second input signal.

36. (Original) A frequency synthesiser as claimed in claim 35, wherein the programmable means is a counter.

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